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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/738,485	KORGER, PETER	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Notice Of Appeal as received on 1/21/2005 and Appeal Brief as received on 3/21/2005.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Drawings

4. New corrected formal drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings in the application are informal drawings, and Applicant is required to provide the Office with formal drawings before the application can issue. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Response to Arguments

5. In view of the appeal brief filed on March 21, 2005, PROSECUTION IS HEREBY REOPENED. However, upon further consideration, a new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, it is not clear how a register stack is stored. Line 2 of claim 15 calls for "means for storing a register stack". However, a register stack is hardware and it is not clear how hardware may be stored.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 5-11, and 13-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Watson, U.S. Patent No. 5,655,132.

10. Referring to claim 1, Watson has taught has taught a circuit comprising:

a) a register stack configured as:

(i) a plurality of segments addressable through a segment address signal. See Fig.4, Fig.5, and Fig.9, for instance, and note that the stack is divided into segments. In general, register addresses ("a") are determined by adding a segment base ("RFG", for instance) and a register offset ("i"). See column 6, line 64, to column 7, line 4. The register address is also a segment address signal because when accessing a particular register, its corresponding segment is also accessed.

(ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address signal. See Fig.9 and note that each segment, in this example, has 32 registers per segment. In addition, registers are accessed through the use of a segment base address (register address signal). See column 6, line 64, to column 7, line 4. Note that the base (RFG, for instance) is used to address a register, and therefore, it is a register address signal.

b) a control circuit configured to:

(i) store a plurality of register states. See column 12, lines 32-45 and note that a plurality of states may be stored in a status register. A first state may be a user state (represented by 0, for instance), while a second state would be a supervisor state (represented by 1, for instance).

(ii) store a segment count signal. See the abstract and note that each instruction which is to access a register includes a relative address field. The relative address specifies which register in the segment, relative to the base, will be accessed. This is a segment count signal because the system will count X registers up from the base in order to determine which register to access.

(iii) present said segment address signal responsive to said plurality of register states, said segment count signal, and said register address signal. See column 7, line 66, to column 8, line 9, and column 12, lines 32-45, and Fig.9, and note that when accessing local registers, the register states will determine the mode (supervisor/user). Depending on the mode, the appropriate segment base address (register address signal) is determined. Once the segment base address is known, a segment count signal (relative address) is added to it to determine the segment address signal (final register address). Therefore, as can be seen, presenting the segment address signal is responsive to each of the aforementioned items.

11. Referring to claim 2, Watson has taught a circuit as described in claim 1. Watson has further taught that at least one of said register states is fixed in a global state. See column 12, lines 32-35, and note global registers in the figures.

12. Referring to claim 3, Watson has taught a circuit as described in claim 1. Watson has further taught that at least one of said register states is fixed in a stackable state. See column 8, lines 52-60.

13. Referring to claim 5, Watson has taught a circuit as described in claim 1. Watson has further taught that the control circuit comprises a status circuit configured to present a gating signal responsive to said register address signal. As shown in column 7, line 4, and column 8, line 8, addition is performed using a register address signal (segment base address) in order to calculate the final register address. Therefore, the signal which causes the addition to occur is the gating signal because the addition signal controls the adder's input signals and the addition signal is given when the register address signal is provided to the adder

14. Referring to claim 6, Watson has taught a circuit as described in claim 5. Watson has further taught that the status circuit comprises a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal. See column 12, lines 32-45, and note that the status bit representing supervisor/user mode is inherently compared to determine what mode the system is in. For instance, the system knows that if the bit is 1, then the system is in user mode, however, if the bit is 0, then the system is in supervisor mode. These are comparisons to 0 and 1 values. In addition, once the mode is known, the appropriate register address signal (base address) is determined. Then in response to the base address, a gating signal (add signal) is given and a final address may be calculated. Therefore, presenting the gating signal is responsive to the register states and register address signal.

15. Referring to claim 7, Watson has taught a circuit as described in claim 5. Watson has further taught that said status circuit comprises a memory device configured to store said

plurality of register states and present said gating signal responsive to said plurality of register states and said register address signal. See column 12, lines 32-45, and note that the status bit representing supervisor/user mode, which is stored in a memory device (status register) is inherently compared to determine what mode the system is in. For instance, the system knows that if the bit is 1, then the system is in user mode, however, if the bit is 0, then the system is in supervisor mode. These are comparisons to 0 and 1 values. In addition, once the mode is known, the appropriate register address signal (base address) is determined. Then in response to the base address, a gating signal (add signal) is given and a final address may be calculated. Therefore, presenting the gating signal is responsive to the register states and register address signal.

16. Referring to claim 8, Watson has taught a circuit as described in claim 17. Watson has further taught that said plurality of logic gates are further configured to present said segment address signal as a predetermined address responsive to said gating signal having a global state. From column 12, lines 32-45, it can be seen that an "add global address" signal or "add local address" signal would be provided. If a global base address is to be added to an offset to present a final address, then the final address is predetermined with respect to the global base address and offset because these values must be known before they are added. Therefore, based on those two values, the final address is predetermined.

17. Referring to claim 9, Watson has taught a circuit as described in claim 18. Watson has further taught that said status circuit comprises a comparator configured to present said gating signal responsive to said plurality of register states and said register address signal. See column 12, lines 32-45, and note that the status bit representing supervisor/user mode is inherently

compared to determine what mode the system is in. For instance, the system knows that if the bit is 1, then the system is in user mode, however, if the bit is 0, then the system is in supervisor mode. These are comparisons to 0 and 1 values. In addition, once the mode is known, the appropriate register address signal (base address) is determined. Then in response to the base address, a gating signal (add signal) is given and a final address may be calculated. Therefore, presenting the gating signal is responsive to the register states and register address signal.

18. Referring to claim 10, Watson has taught a method of controlling a register stack comprising the steps of:

a) comparing a register address with a plurality of register states to present a gating signal. See column 12, lines 32-45 and note that the relative offset is compared to see if it corresponds to a global register, a local user register, or a local supervisor register. Once it is determined what type of register is to be accessed, the corresponding base address is sent to an adder (for adding to the relative offset - see column 7, line 4, for instance) and a gating signal would inherently tell the adder to proceed with adding. This signal is a gating signal because it controls the accessing of the adder input signals (base and offset).

b) gating a segment count with said gating signal to present a segment address. Again, from column 7, line 4, it can be seen that the relative address (segment count) is gated into the adder when the adder is told to add. At the same time, a segment address (base address) would inherently be presented to the adder for adding and determining a final register address. It should be realized that the offset (relative address) is a segment count because the system will count X registers up from the base in order to determine which register to access.

c) addressing said register stack with said register address and said segment address. From column 7, line 4, it can be seen that the final address is equal to the base (segment address) plus the offset (register address). Therefore, the register stack is addressed with the segment and register addresses).

19. Referring to claim 11, Watson has taught a method as described in claim 10. Watson has further taught that step (a) further comprises the substeps of:

a) presenting a signal communicating said plurality of register states. Clearly, when the state is determined (global, local user, or local supervisor), a signal would inherently be used to specify it. Otherwise, determining the state would serve no purpose.

b) selecting one of said plurality of register states as said gating signal based upon said register address. Based on the state, different base addresses are used in the calculation of a final address. For instance, if a first relative address is determined to be of a global type, then this determination will result in selecting a global base address for addition. However, if a second relative address is determined to be of a local user type, then this determination will result in selecting a local user base address for addition. Therefore, the state acts as a gating signal.

20. Referring to claim 13, Watson has taught a method as described in claim 10. Watson has further taught the step of incrementing said segment address in response to a push instruction. See Fig.8, column 1, lines 35-44, and column 11, line 65, to column 12, line 18, and note that as each new task is encountered, it gets a new portion of the register stack allocated to it, with a segment base address that is larger than the previous segments address. Therefore, in response to a push (adding information to the stack), the segment address is incremented.

21. Referring to claim 14, Watson has taught a method as described in claim 13. Watson has further taught the step of decrementing said segment address in response to a pop instruction. See Fig.8, column 1, lines 35-44, and column 11, line 65, to column 12, line 18, and note that as each new task is encountered, it gets a new portion of the register stack allocated to it, with a segment base address that is larger than the previous segments address. On the other hand, when tasks are finished, its register space is deallocated and the previous segments address is reloaded such that it specifies the current segment. This reloading in effect decrements the segment address. Therefore, in response to a pop (removing information from the stack), the segment address is incremented.

22. Referring to claim 15, Watson has taught a circuit comprising:

a) means for storing a register stack configured as:

(i) a plurality of segments addressable through a segment address. See Fig.4, Fig.5, and Fig.9, for instance, and note that the stack is divided into segments. In general, register addresses ("a") are determined by adding a segment base ("RFG", for instance) and a register offset ("i"). See column 6, line 64, to column 7, line 4. The register address is also a segment address because when accessing a particular register, its corresponding segment is also accessed.

(ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address. See Fig.9 and note that each segment, in this example, has 32 registers per segment. In addition, registers are accessed through the use of a segment base address (register address signal). See column 6, line

64, to column 7, line 4. Note that the base (RFG, for instance) is used to address a register, and therefore, it is a register address.

b) means for storing a plurality of register states. See column 12, lines 32-45 and note that a plurality of states may be stored in a status register. A first state may be a user state (represented by 0, for instance), while a second state would be a supervisor state (represented by 1, for instance).

c) means for storing a segment count. See the abstract and note that each instruction which is to access a register includes a relative address field. The relative address specifies which register in the segment, relative to the base, will be accessed. This is a segment count signal because the system will count X registers up from the base in order to determine which register to access.

d) means for presenting said segment address responsive to said register address and said plurality of register states and said segment count. See column 7, line 66, to column 8, line 9, and column 12, lines 32-45, and Fig.9, and note that when accessing local registers, the register states will determine the mode (supervisor/user). Depending on the mode, the appropriate segment base address (register address signal) is determined. Once the segment base address is known, a segment count signal (relative address) is added to it to determine the segment address signal (final register address). Therefore, as can be seen, presenting the segment address signal is responsive to each of the aforementioned items.

23. Referring to claim 16, Watson has taught a circuit as described in claim 1. Watson has further taught that said control circuit comprises a counter configured to present said segment count signal. As described in the abstract, the instruction's relative address field presents the

segment count, i.e., the number of registers away from the base address at which the register to be accessed is located. Therefore, since it provides a count, it is a counter.

24. Referring to claim 17, Watson has taught a circuit as described in claim 5. Watson has further taught that said control circuit comprises a plurality of logic gates configured to present said segment address signal responsive to said gating signal and said segment count signal. Note from column 7, line 4, and column 8, line 8, that a final register address (segment address signal) is presented after adding an offset and a base. The adder would comprise a plurality of logic gates and would take the segment count signal (offset) as an input. Then a gating signal would tell the adder to add when both the base and offset have been provided. As a result, the gates present the final address in response to the gating signal and segment count signal.

25. Referring to claim 18, Watson has taught a method as described in claim 10. Watson has further taught presenting said segment address as a predetermined address responsive to said gating signal having a global state. From column 12, lines 32-45, it can be seen that an "add global address" signal or "add local address" signal would be provided. If a global base address is to be added to an offset to present a final address, then the global base address is predetermined with respect to the time at which it is added to the offset to form the final address/ That is, the global base address must be known before they are added so that the addition may occur. Therefore, the segment address is predetermined.

26. Referring to claim 19, Watson has taught a method as described in claim 10. Watson has further taught storing said register states prior to said comparing. See column 12, lines 32-45 and note that states are stored in the status register.

27. Referring to claim 20, Watson has taught a method as described in claim 10. Watson has further taught storing said segment count prior to said gating. The segment count (offset/relative address) is stored within the instruction itself before it is selected and propagated in any fashion. Consequently, the segment count is stored prior to the gating.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson, as applied above, in view of Guttag, U.S. Patent No. 4,402,042.

30. Referring to claim 4, Watson has taught a circuit as described in claim 1.

a) Watson has further taught that the register stack comprises a first portion disposed within a processor and configured as at least one segment of said plurality of segments. See Fig.2 and note that Fig.2 represents a processor which includes a register file.

b) Watson has not taught that the register stack comprises a second portion disposed external to said processor and configured as at least one segment of said plurality of segments. However, Guttag has taught a system in which registers may be external to the CPU. See column 4, line 64, to column 5, line 3. As disclosed, this allows for increased programming flexibility and for faster response to interrupts. Of course, as is known, it is also beneficial to have registers on-chip as they may be accessed very quickly by the processor. Therefore, in order to realize both

advantages, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watson such that a portion of the registers are external to the CPU.

31. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson, as applied above.

32. Referring to claim 12, Watson has taught a circuit as described in claim 10. Watson has not explicitly taught setting said plurality of register states in response to a reset handler operation. However, Official Notice is taken that the use of reset handlers is well known and accepted in the art. That is, reset handlers are used to reset/restore the system in some manner. Clearly, if a reset is to occur in Watson, due to an error, or power outage, then before any registers can be accessed, the segment base addresses must be set ahead of time. And, in this determines the states. For instance, if the global base is set to address 0, then the global state corresponds to a range of registers starting at address 0. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Watson to include a reset handler for setting the states of the system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
May 10, 2005

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